(b)

MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1 2022/2023 (TERM ID 2210)

EEE4166 – DIGITAL INTEGRATED CIRCUIT

(All sections / Groups)

7 FEBRUARY 2023
9.00 a.m – 11.00 a.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This question paper has 4 questions only.
2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please print all your answers in the Answer Booklet provided.

Formulas:

Ideal diode equation: $I_D = I_S(e^{\frac{V_D}{\phi_T}} - 1)$

$$V_T = V_{TO} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

saturation:

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

linear:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right)$$

unified model:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DSAT} - \frac{{V_{DSAT}}^2}{2}\right)(1 + \lambda V_{DS})$$

$$t_P = \frac{C_L\frac{V_{SWING}}{2}}{I_{AVG}}$$

$$t_P = 0.69\, R_{eq}C_L$$

$$P_{dyn} = C_L{V_{DD}}^2 f$$

Question 1

(a) A simple diode circuit is shown in Figure Q1.

(i) Assuming a silicon diode D1 with $V_{D(on)} = 0.7$ V, determine current (I_D) and voltage on R1.

(ii) If the voltage source V1 is changed to 5 V, what is the new value for the diode current (I_D)?

[4+2 marks]

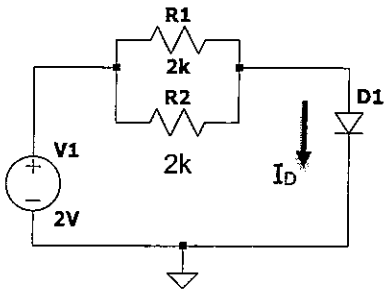

Figure Q1

(b) An NMOS transistor has aspect ratio of W/L = 4/3 with parameters are given as following: threshold voltage, $V_{T0} = 0.43$ V, $-2\varphi_F = 0.8$ V, body effect coefficient, $\gamma = 0.4\ \sqrt{V}$ and $k_n' = 115\ \mu A/V^2$. The NMOS transistor is operating with $V_{SB} = 1.6$ V, $V_{GS} = 3$ V and $V_{DS} = 3$ V.

(i) Determine the mode of operation of this transistor.

(ii) Calculate the drain current, I_D of the transistor.

(iii) Re-calculate the drain current, I_D if the size of the transistor, W/L = 10.

(iv) Comment on the relationship between part (ii) and (iii).

[4+2+2+2 marks]

(c) Calculate the diffusion capacitance, C_{diff} for a NMOS transistor with the given below values:

Width, W = 5 μm, length, $L_S = L_D = 2$ μm, and constants given as junction capacitance, $C_j = 3.2 \times 10^{-4}$ F/m^2 and junction sidewall capacitance, $C_{jsw} = 7.2 \times 10^{-10}$ F/m.

[5 marks]

(d) Understanding the second-order effects and their impact on an actual MOS transistor is essential in the design of digital circuits.

(i) Describe the latch-up effect.

(ii) Suggest a method to minimize the latch-up effect.

[2+2 marks]

Continued...

Question 2

(a) A Voltage Transfer Characteristics (VTC) graph for an inverter is shown in Figure Q2.

(i) Redraw the VTC graph and label the critical voltages, V_{IL}, V_{IH}, V_{OL}, V_{OH} and V_M on the graph.

(ii) Based on the graph, estimate the values of the critical voltages (V_{IL}, V_{IH}, V_{OL} and V_{OH}) and calculate the low noise margin, NM_L and high noise margin, NM_H.

[5+8 marks]

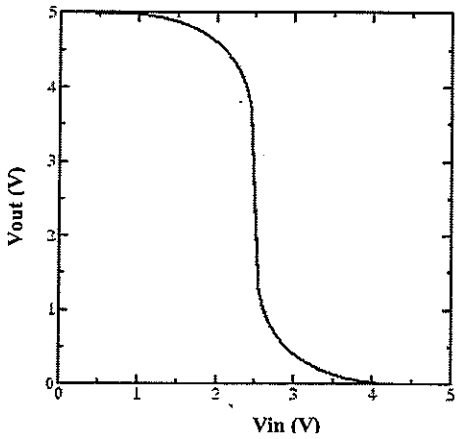

Figure Q2

(b) Given the function F below:

$$F = (\overline{C.B}) + A$$

(i) Design a static CMOS gate realization of this function F with minimum transistor count. Both the input and inverted input ports are available for implementation.

(ii) From the design in Part (i), compute the W/L ratios of the transistors so that the output resistance is the same as an inverter with $(W/L)_{NMOS} = 3$ and $(W/L)_{PMOS} = 5$.

[8+2 marks]

(c) In sequential logic, Voltage Controlled Oscillator (VCO) is used as an astable multivibrator. Describe the operation of the VCO emphasizing on the current starved inverter.

[2 marks]

Continued...

Question 3

(a) Referring to Figure Q3(a) below, **design** the Emitter-Coupled Logic (ECL) OR/NOR gate of the circuit.
It has two inputs. The desired collector currents are I_{C1} = 3 mA and V_{EE} = -5 V. At logic high, V_{OR} = -0.7 V, V_{NOR} = -1.5 V and $v_a = v_b$ = -0.7 V. Assume V_{BE} = 0.7 V and β = 50.

[11 marks]

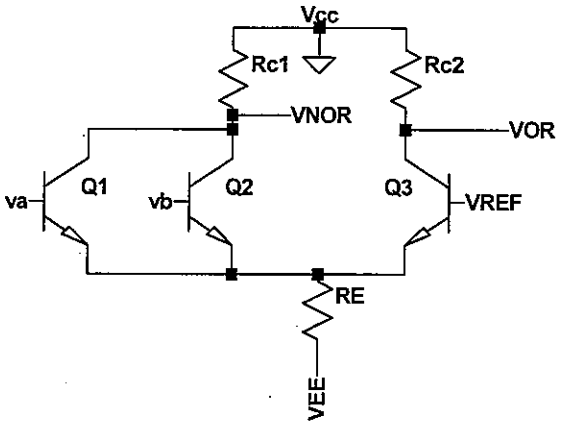

Figure Q3(a)

(b) Design a BJT inverter as shown in Figure Q3(b), to drive four identical inverters (N = 5) and to give V_{OH} = 3.5 V and NM_L = 0.4 V. The transistor has $I_{C(sat)}$ = 5mA, β = 50, $V_{BE(cut\text{-}in)}$ = 0.6 V and $V_{BE(sat)}$ = 0.8 V. The supply voltage V_{CC} = 5 V.

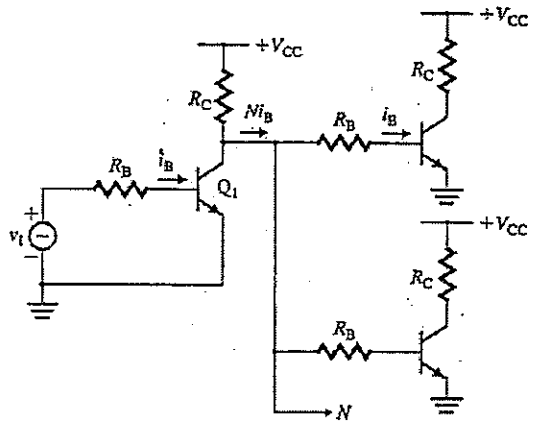

Figure Q3(b) [14 marks]

Continued...

Question 4

(a) Implement the following function, Y using static CMOS gates.

$$Y = \overline{A + B} + C$$

[8 marks]

(b) Given the load capacitance, C_L = 100 pF, voltage supply, V_{DD} = 3 V and clock frequency, f_{clk} = 500 MHz. Assume that the input signals are random. Based on the circuit drawn in Part (a),

(i) Determine the dynamic power consumption, P_{dyn} of the circuit.
Hint: Use a truth table

(ii) Assume the leakage current is 3 nA and the propagation delay is 1 ns, calculate the Power-Delay-Product (PDP) of the circuit.

[7+3 marks]

(c) Figure Q4 shows the trend in power dissipation as technology (micron) scales down towards 0.1 micron.

(i) Comment on the graph in Figure Q4.

(ii) Recommend TWO methods to reduce the power dissipation.

[3+4 marks]

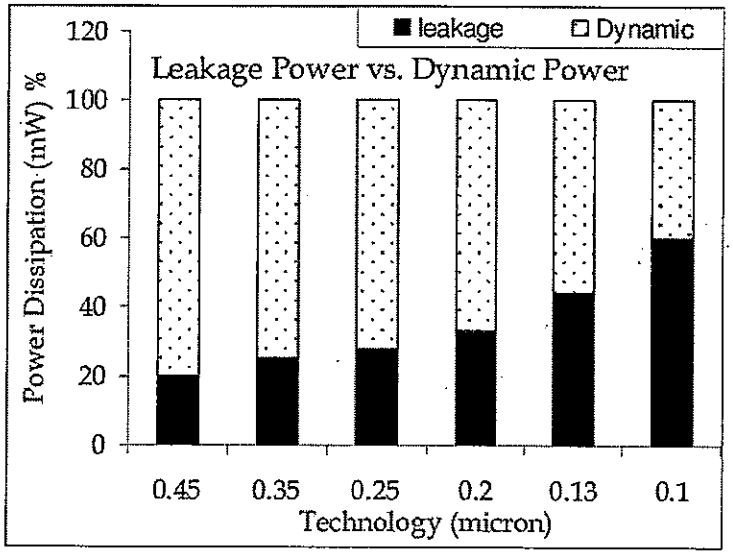

Figure Q4

End of Paper.